2.7 A 40Gb/s Transimpedance-AGC Amplifier with 19dB DR in 90nm CMOS

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The development of multimedia communications has demanded for multi-Gb/s data-transmission systems. Such systems require high-speed front-end amplifiers in the receive paths. The amplifiers must deal with tiny input signals, providing output signals as large as hundreds of millivolts for the subsequent clock and data recovery. In this paper, the design and experimental verification of a 40Gb/s transimpedance-AGC (TIA-AGC) amplifier realized in 90nm CMOS technology are described.

Figure 2.7.1 depicts the architecture of the TIA-AGC amplifier. The AGC loop is used to keep the intermediate stages operate linearly, reducing jitter and pulse-width distortion at high input currents. To ensure that the CML buffer completely switches at high speed, the signal swing entering the buffer is maintained as $400mV_{pp}$ per side by the AGC loop. The buffer thus acts as a soft limiter and provides an output swing of $260mV_{pp}$ per side on the 25Ω equivalent loads.

The trade-offs between input resistance, noise, and voltage headroom pose challenges in the design of high-speed TIAs. Considering the common-gate (CG) TIA depicted in Fig. 2.7.2(a), the bias current needs to be large to obtain a low input resistance, especially when M_1 is made narrow to minimize C_{in}. This not only raises the noise from the tail current (I_{SS}), but results in a small R_{L1} due to the headroom limitation, which in turn worsens the noise from the following stage (A_2). To alleviate these issues to some extent, a feedback resistor, R_F, is inserted as shown in Fig. 2.7.2(b), and R_{L1} and I_{SS} are increased and decreased by m times, respectively. In order not to make the input-referred noise worse, the sum of the noise from mR_{L1} and R_F is made equal to that from R_{L1}, which requires that $R_F \geq mR_{L1}/(m-1)$. With g_{m1} decreased by m times due to the $1/m$ bias current, the condition for the input resistance in Fig. 2.7.2(b) to be smaller than that in Fig. 2.7.2(a) is given by:

$$Z_{in} < \left(\frac{g_{m1}}{m} + \frac{m-1}{mR_{L1}} g_{m1} R_{L1} A_2\right)^{-1} \leq g_{m1}^{-1} \Rightarrow A_2 \geq 1$$

The condition of unity gain is not difficult to meet even at such high speed. For A_2>1, the CG TIA with feedback provides a lower input resistance with lower power compared to the conventional CG TIA. Besides, the input-referred noise due to the tail current and the following stage (A_2) becomes lower, increasing the sensitivity. In the proposed design, m=1.5 and A_2=2, resulting in 25% decrease in input resistance and 33% reduction in power.

The circuit of the TIA is depicted in Fig. 2.7.3. Source followers are inserted between the feedback resistors and the second stage, avoiding the former to load the latter. To take the advantages of the feedback, the loop gain must be maintained up to high frequencies, necessitating some broadband techniques. To extend the bandwidth efficiently when the parasitic capacitance is unevenly distributed between the present and the next stage, the input and output port of the network formed by L_1-R_1-L_2 in [1] are simply interchanged, resulting in the inductive series-shunt peaking configuration. Since this network exhibits 3 resonance frequencies ($\omega_{1,2,3}$ in Fig. 2.7.3) and is the reversed version of that in [1], it is called the reversed triple-resonance network (RTRN).

The equivalent model of the RTRN is deduced in Fig. 2.7.4. The parasitic capacitance is assumed to be unevenly distributed, with $C(1-\alpha)/2$ on the present stage and $C(1+\alpha)/2$ on the next. The first and second resonance frequencies are easily observed in the expression of Z_{tot} (in Fig. 2.7.4) and the third one occurs at which the imaginary part of Z_{tot} becomes purely zero. The first resonance frequency can be chosen so that $\omega_1 = 1/\sqrt{LC}$ and $|Z_{tot}(j\omega_1)| = R_1$ [1]. This results in the following design:

$$L_1 = (1-\alpha)^2 CR_1^2/4,\ L_2 = (1-\alpha)CR_1^2/2$$

By substituting them into the expressions of the 3 resonance frequencies, the results in Fig. 2.7.4 can be obtained. Interestingly, it can be proved that the impedance of the TRN [1] can be simplified to be of the same form, except that a is replaced by $-\alpha$. By following the same procedure as that described above, $L_{1,2}$ and $\omega_{1,2,3}$ in the TRN can be obtained. As expected, their expressions are similar to those in the RTRN, except that α is replaced by $-\alpha$.

The above results lead to the direct comparison of RTRN with TRN, under the general condition that the parasitic capacitance is unevenly distributed. As plotted in Fig. 2.7.4, the third resonance frequency, ω_3, increases faster in the RTRN than in the TRN when α increases. Besides, the impedance of the RTRN at ω_3 can be calculated by:

$$|Z_{tot}(j\omega_3)| = |\mathrm{Re}\{Z_{tot}(j\omega_3)\}| = \left|\frac{1+(\omega_3/\omega_1)^2(1-\alpha)^2/4}{1-(\omega_3/\omega_1)^2}\right| R_1$$

For α=0.2, $|Z_{tot}(j\omega_3)|$ equals to $1.5R_1$ in the RTRN and $0.9R_1$ in the TRN. In other words, the gain at ω_3 is 4dB larger in the RTRN than in the TRN. For larger values of α, the difference becomes even more significant. The results of higher ω_3 and higher gain at this frequency imply that the RTRN is more capable of providing gain at high frequencies, especially for cases of unevenly distributed capacitances. The peaking at ω_2 is of concern in the RTRN when α becomes large. Fortunately, the finite Q of inductors reduces the peaking, allowing the inductors to be realized as narrow traces to save area and to facilitate signal routing. In the proposed design, the trace width is 1.6μm, which results in reducing the peaking to <1dB.

With the gain of 500Ω, the TIA needs post amplification to amplify the signals to CML levels. The circuit of the following VGA is depicted in Fig. 2.7.5. In contrast to the Gilbert cell, the gates of $M_{3,4}$ are tied to a fixed bias rather than the input, reducing the loading on the previous stage. Since $M_{3,4}$ are used only for current steering, their size is 1/5 times that of $M_{1,2}$. This further lowers the capacitances at the output nodes, allowing high-speed operation. The two gain stages following the VGA are realized as Cherry-Hooper amplifiers with active feedback [2]. To reduce the area, all the shunt-peaking inductors are made by stacked spirals.

The TIA-AGC amplifier is fabricated in 90nm CMOS and tested on a probe station. The average input resistance is 100Ω differential obtained from the measured S_{11}. Due to the limiting nature of the output buffer, the small-signal gain is measured by 40Gb/s 2^{31}–1 PRBS input with $220\mu A_{pp}$ swing, resulting in a non-limited output swing of $220mV_{pp}$ per side. The differential gain is thus equal to 2kΩ.

Figure 2.7.6 shows the single-ended output eyes for 40Gb/s 2^{31}–1 PRBS input. The output swing remains $260mV_{pp}$ per side for an input dynamic range of 19dB, from $440\mu A_{pp}$ to $4mA_{pp}$. The output jitter is less than $10ps_{pp}$, while the input data suffers from an intrinsic jitter of 6 to $7ps_{pp}$.

The integrated output noise of the amplifier is observed on the oscilloscope with the input signal source disabled. By using the histogram function, the corresponding input referred noise is measured to be $3.6\mu A_{rms}$.

Figure 2.7.7(a) shows the die micrograph and Fig. 2.7.7(b) summarizes the measured performance. The amplifier including the output buffer consumes 75mW from a 1.2V supply.

Acknowledgements:
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References:

[1] S. Galal and B. Razavi, "40Gb/s Amplifier and ESD Protection Circuit in 0.18μm CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 480–481, Feb., 2004.

[2] S. Galal and B. Razavi, "10Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18μm CMOS Technology," *ISSCC Dig. Tech. Papers*, pp. 188–189, Feb., 2003.

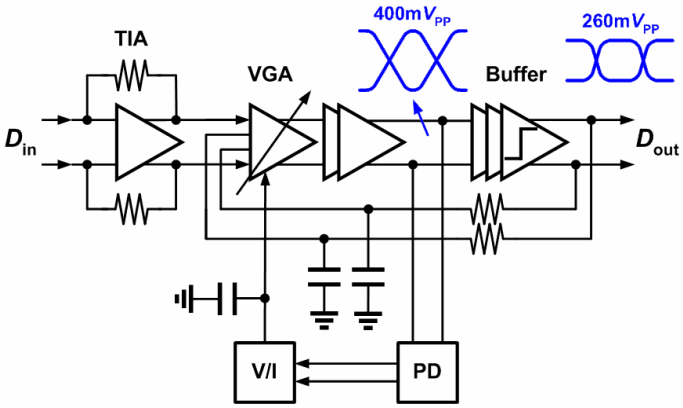

Figure 2.7.1: Architecture of the 40Gb/s transimpedance-AGC amplifier.

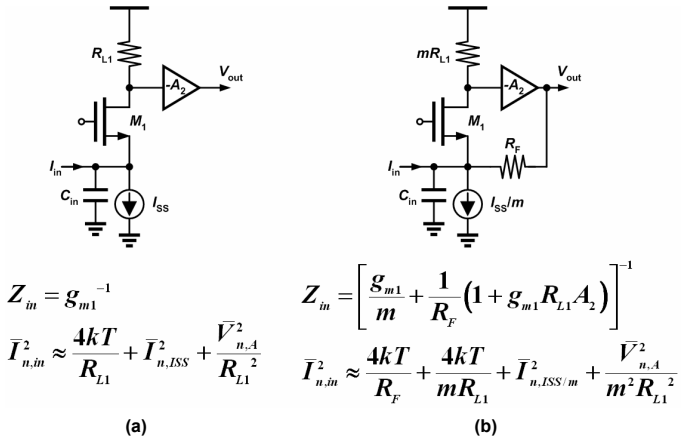

Figure 2.7.2: (a) Conventional CG TIA (b) Proposed CG TIA with resistor feedback.

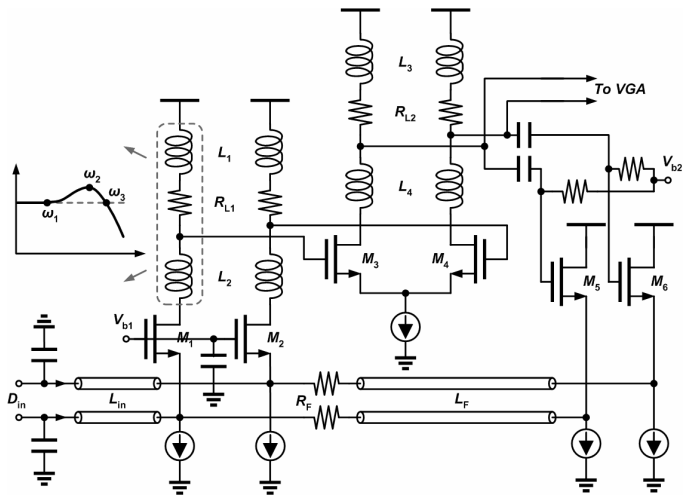

Figure 2.7.3: Circuit topology of the proposed TIA.

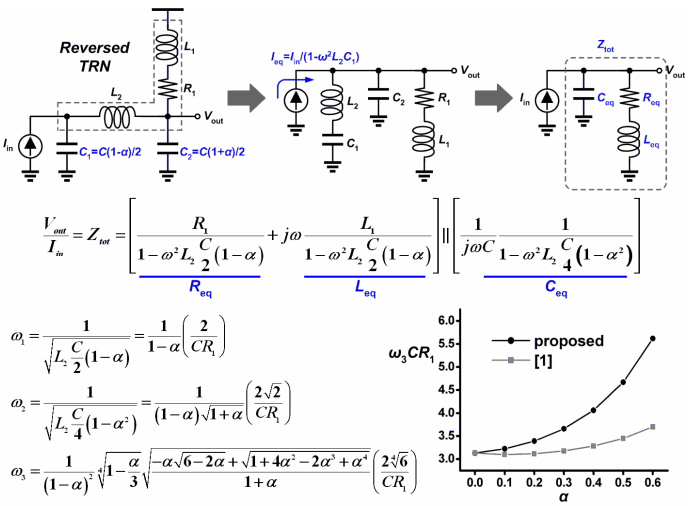

Figure 2.7.4: Frequency response of the reversed triple-resonance network (RTRN).

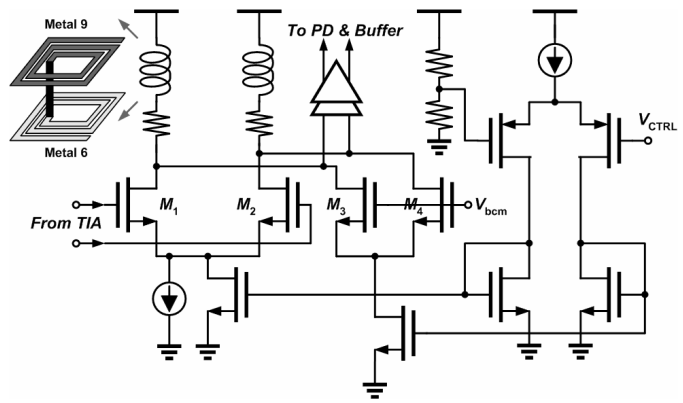

Figure 2.7.5: Circuit topology of the proposed VGA.

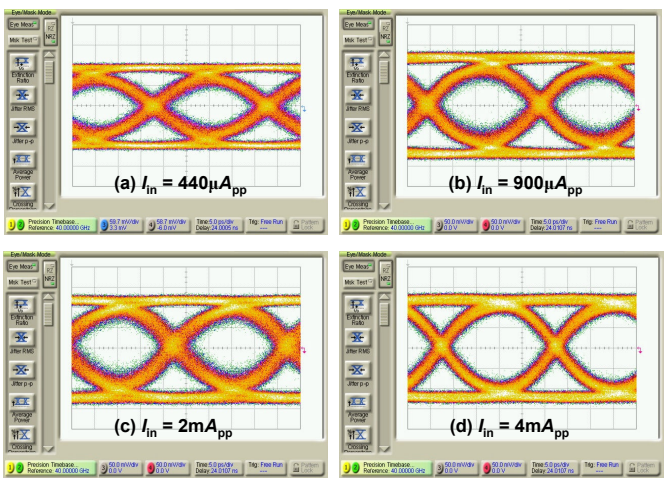

Figure 2.7.6: Measured 40Gb/s 2^{31}–1 single-ended output eyes for different input swings. (H scale: 5ps/div, V scale: 60mV/div in (a) and 50mV/div in others).

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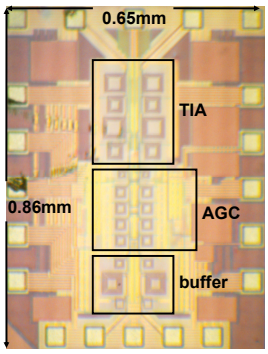

(a)

Technology	90nm CMOS
Data Rate	40Gb/s
Small Signal Gain	2kΩ
Output Swing	520m$V_{pp\text{-}diff}$
Dynamic Range	19dB ($440\mu A_{pp}$– $4mA_{pp}$)
Peak-to-Peak Jitter	< 10ps
Input Referred Noise	$3.6\mu A_{rms}$
Overall Power	75mW
Supply Voltage	1.2V
Area	$0.56mm^2$

(b)

Figure 2.7.7: (a) Die micrograph (b) Measured performance summary.

